What is claimed is:

1. An apparatus for controlling a self refresh operation in a synchronous semiconductor memory device, comprising:

a self refresh pulse signal generation block for generating a self refresh pulse signal, a self refresh entry signal and a self refresh mode clock enable signal in response to a clock enable signal, a self refresh signal, a self refresh end signal and a test mode signal, wherein the self refresh pulse signal is generated during the inactivated period of the clock enable signal by using the test mode signal;

a normal mode clock signal generation block for generating a normal mode clock signal and a counter reset signal in response to the clock enable signal, the self refresh mode clock enable signal, a test mode signal and the self refresh signal; and

an internal row address counter in response to the self refresh pulse signal and the counter reset signal for generating internal addresses for use in the self refresh operation.

2. The apparatus as recited in claim 1, further comprising a '0' address detector for detecting the internal address of all '0's.

3. The apparatus as recited in claim 1, wherein the self

refresh pulse signal generation block includes a pulse width controller in response to the self refresh pulse signal and the test mode signal for generating a pulse width controlled self refresh pulse signal.

4. The apparatus as recited in claim 1, wherein the self refresh pulse signal generation block includes a self refresh mode exit block in response to the pulse width controlled self refresh pulse signal, the self refresh mode clock enable signal and the self refresh end signal for generating a self refresh exit signal.

5. The apparatus as recited in claim 1, wherein the self refresh pulse signal generation block includes a self refresh signal generator for generating the self refresh signal in response to the self refresh exit signal and the self refresh entry signal.

6. The apparatus as recited in claim 1, wherein the self refresh pulse signal generation block includes a self refresh pulse generator for generating the self refresh pulse signal in response to the self refresh signal.

7. The apparatus as recited in claim 1, wherein the normal mode clock signal generation block includes:

a test mode controller for generating a first output signal and the counter reset signal in response to the test

mode signal, the self refresh mode clock enable signal and the self refresh signal;

a normal mode clock enable buffer for generating a normal mode clock enable signal in response to the first output signal and the clock enable signal; and

a clock buffer for generating the normal mode clock signal in response to the normal mode clock enable signal.

8. The apparatus as recited in claim 4, wherein the self refresh mode exit block includes:

an RS-LATCH for generating a second output signal in response to the pulse width controlled self refresh pulse signal and the self refresh end signal; and

a first logic gate for outputting the self refresh exit signal in response to the self refresh mode clock enable signal and the second output signal.

9. The apparatus as recited in claim 7, wherein test mode controller includes:

a second logic gate for outputting the counter reset signal in response to the test mode signal and the self refresh mode clock enable signal; and

a third logic gate for outputting the first output signal in response to the self refresh signal and the counter reset signal.